THE DESIGN OF HIGH-SPEED ALL-TRANSISTOR LOGIC CIRCUITS

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INTRODUCTION

The development of silicon transistor type 2N709, which has a typical charge storage time constant of three nanoseconds, makes possible simple logic circuits having less than five nanoseconds delay per stage with less than five milliwatts of power dissipation per stage. Furthermore, these circuits allow complete logic stages to be placed in single transistor cans by using special packaging techniques. This not only decreases size, but also increases the operating speed of the logic circuit by reducing lead inductance and stray capacitance. The special packaging is a reliable and readily available miniaturization technique, whereby several transistor chips are put in one TO-5 transistor can.

This paper describes a basic logic circuit capable of operation at VHF, which may be used to form many different logic functions.

COMPUTER DESIGN CONSIDERATIONS

Three design goals should be considered. First, reduced distance between circuits by miniaturizing circuit construction is important. This design goal minimizes pulse transmission difficulties due to lead inductance and stray capacitance which limit operating speed. Miniaturization increases the importance of low power dissipation, keeping temperature rise inside the circuit parts as low as possible. Low power dissipation implies the need for an active device with low capacitances, low storage time delays and a large gain-bandwidth product at low currents and voltages.

A second design goal is to minimize the time delay per stage by reducing the number of components in the logical design. Non-logic functions, such as polarity inversion, must be eliminated whenever possible. Also, both a logical OR and a logical AND circuit using common polarities must exist. For example, Figure 1

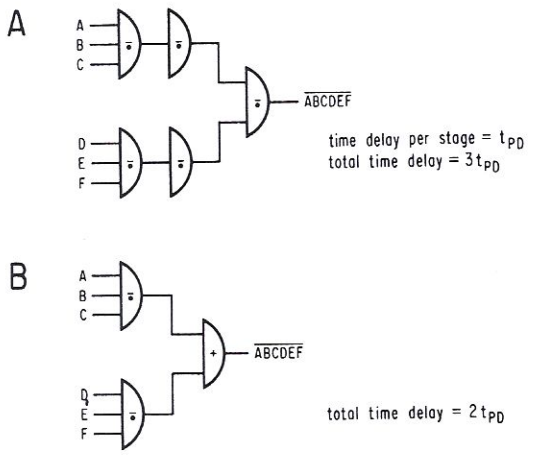

Fig. 1. Multiple input NAND gates using a) NAND gates only; b) NAND and OR gates.

shows a multiple input NAND gate using (a) NAND gates only, and (b) both NAND and OR gates. Multiple input means more inputs than the fan-in of one NAND gate. The figure shows that having both types of gates reduces the time delay and physical size of a multiple input gate.

A third design goal is to reduce the voltage and current changes in the circuits as much as possible, so that the charging times of the capacitance and inductance are minimized. This means that low-level logic of some kind is desirable.

BASIC CIRCUITS

This section describes a logic gate which is used for low power circuits and shows an evolution to a simpler and faster low power form.

LLL Gate

Figure 2a shows a Low Level Logic (LLL) positive NAND gate. It has the advantage of relatively low power operation with only one power supply. However, it has some disadvantages.

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First, it uses three different kinds of parts; fewer kinds of parts would simplify size reduction and construction which, in turn, reduces manufacturing cost.

Second, the LLL gate is slow, because there is no path for turn-off base current from the inverter. The storage time may be decreased by connecting the base of the inverter through a resistor to a negative supply, but this increases the number of parts, the power dissipation, and the number of required power supplies.

T^2L Gate

Beeson and Ruegg* have suggested a form of All Transistor Logic which does not have the disadvantages of LLL, but retains its advantage of low power capability. The NAND gate is shown in Figure 2b. They have called it Transistor Transistor Logic (TTL or T^2L) because it uses transistor gates in addition to the inverter transistor.

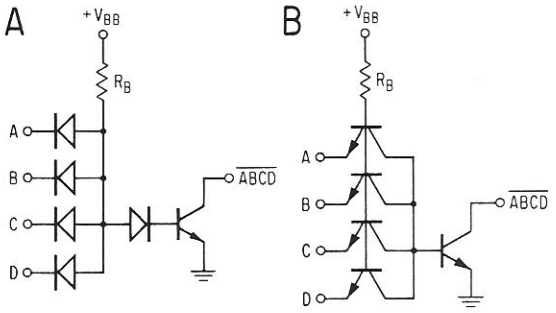

Fig. 2. Two basic NAND circuits. a) LLL, and b) T^2L.

The static operation of the T^2L NAND gate is explained by Figure 3. Figure 3a shows the conditions when the inverter transistor is saturated. The only path for the base current of T2 is into the base of T3. The collector voltage of T1 is typically 800 millivolts in this case, since the drop across T2 is typically 10 millivolts and the base voltage of T3 is about 800 millivolts. Figure 3b shows the conditions when the inverter transistor is not conducting current.

*New Forms of All Transistor Logic, Solid State Circuit Conference, March 1962, Fairchild Paper TP-21.

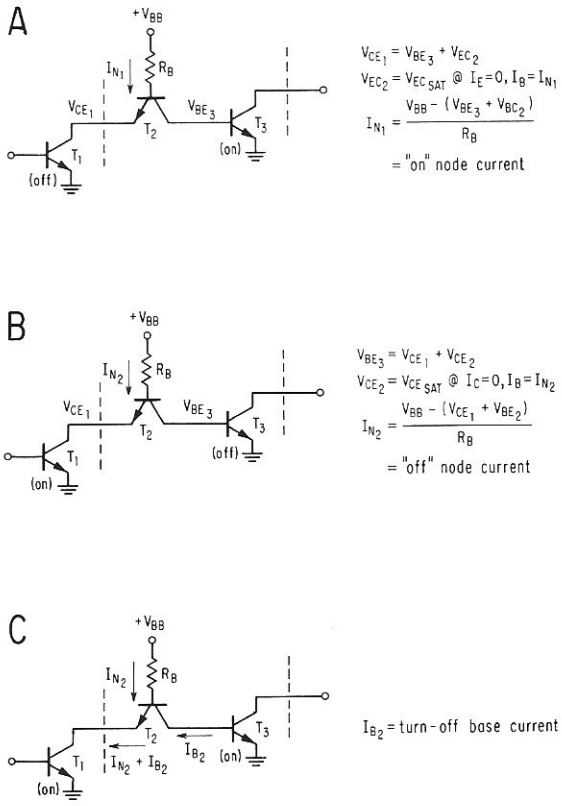

Fig. 3. Static operation of T^2L NAND gate. a) ON, b) OFF, and c) turn off current.

All the base current of T2 flows into the collector of T1. The drop across T2 in this case is typically 80 millivolts, so if the collector voltage of T1 is 100 to 300 millivolts, the base voltage of T3 is no more than 400 millivolts. The collector current of T3 will be negligible for base voltages less than 600 millivolts, so T3 is cut off. The typical base and collector voltages given here apply for the 2N709.

Figure 3c shows that the use of transistor gating instead of diode gating provides a path for turn-off base current from the inverter transistor. When T1 turns on, its collector current is the emitter current of T2, and the emitter current of T2 is in the normal direction. The turn-off base current of T3 is the collector current of T2, which can approach the product of I_{N2} and the normal current gain of T2. The magnitude of the turn-off base current of T3 depends on how much current T1 can collect and maintain a low collector voltage.

Note that the gating transistor T2 is always saturated, either in the normal direction or the inverted direction. That is, when the emitter current is in the forward direction (T3 off), the collector current is zero. When the collector current is in the inverted direction, the emitter current is zero. Thus, there should be little, if any, storage delay, so it is reasonable to expect the propagation delay through the NAND gate to be essentially that of the inverter alone. To verify this, a ring oscillator was built using the T^2L gate. A ring oscillator is an odd number of inverters where the output of the last inverter is the input of the first. If the total delay time of all the inverters is more than the rise and fall time of each inverter, the ring is unstable, and the period of oscillation of each inverter is twice the product of the average propagation delay of each inverter and the number of inverters. For a three-volt supply and a three-milliampere on node current, the average propagation delay using all 2N709 transistors was 2.7 nanoseconds. Then the gating transistors were replaced by direct wires and the supply reduced to 2.2 volts to maintain the same node currents. The average propagation delay decreased to 2.4 nanoseconds. This means the gating transistor was increasing the delay by only 0.3 nanoseconds.

The disadvantage of the T^2L gate compared to the LLL gate is that fan-out, in a worst case situation, can be reduced by current robbing. This is shown in Figure 4a. The base voltage of T4 is larger than the base voltages of the other on inverters if collector current of T4 is larger than that of the other inverters. The difference causes a robbed current, I*, to flow into the gates associated with the inverters with the lower base voltages. Since this current flows into the emitter of each gating transistor in the inverted direction, it will not exceed the product of the base current and the inverted current gain of the gating transistor. In practice, using the 2N709, if the spread in base voltages is as large as 80 millivolts, the robbed current is within 10% of its maximum. Figure 4b is used to calculate the effect of this robbed current on fan-out.

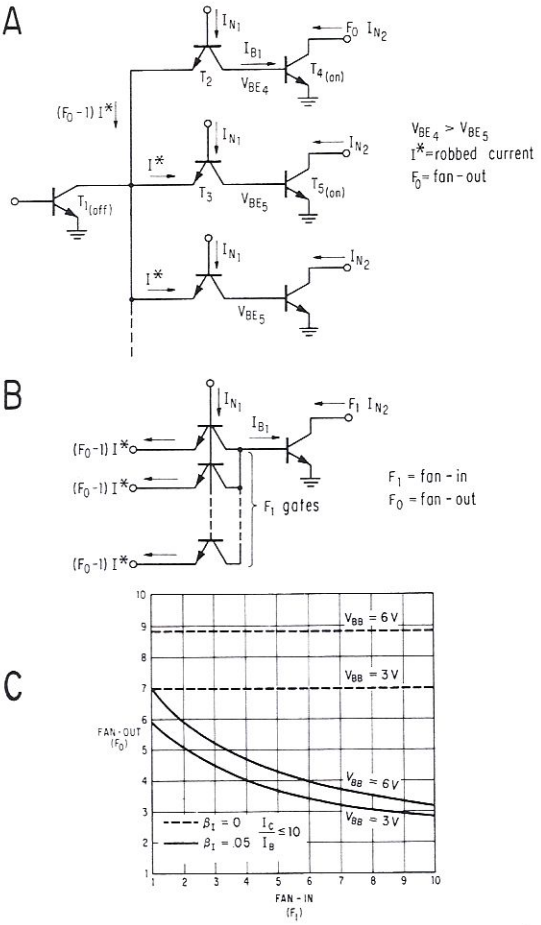

Fig. 4. The effect of current robbing in T^2L NAND gate. a) reduced fan-out, b) worst case, and c) fan-out vs fan-in.

For worst case design, the minimum on base current is given by:

$$I_{B1} = I_{N1} - F_1 (F_O - 1) I^*$$

assume $I^* \leq \beta_I I_{N1}$

$$I_{B1} > I_{N1} \left[1 - F_I (F_O - 1) \beta_I\right]$$

$$I_{C1} = I_{N2} F_O = \beta_C I_{B1}$$

where β_C = circuit current gain

$$F_O > \frac{I_{N1}}{I_{N2}} \beta_C \left[1 - F_1 (F_O - 1) \beta_I\right] \text{ or}$$

$$F_O > \frac{I_{N1}}{I_{N2}} \beta_C \frac{1 + \beta_I F_1}{1 + \beta_I F_1 \beta_C \frac{I_{N1}}{I_{N2}}}$$

where. F_O = fan-out, F_I = fan-in, β_C = ratio collector to base current, β_I = inverted current gain, I_{N1} = on node current, I_{N2} = off node current.

Using values of .05 and 10 for β_I and β_C, the curves of Figure 4c can be calculated. The upper two curves correspond to the cases where current robbing is negligible. For a 3 V supply and a fan-in of four, worst case design, accounting for possible current robbing, reduces the fan-out by 40%. While this is a large percentage, the available fan-out is still large enough to be usable in many applications.

PROPAGATION DELAY OF THE T^2L NAND GATE

A ring oscillator was built to determine what effects fan-out and capacitance have on delay, and also to determine what current levels yield the shortest delay times. This ring was made with FSP-352-1's, which are three-input NAND gates with extra transistors to enable operation as half a directly coupled flip-flop. Figure 5a is a schematic of an FSP-352-1, and Figure 5b is a block diagram of the oscillator.

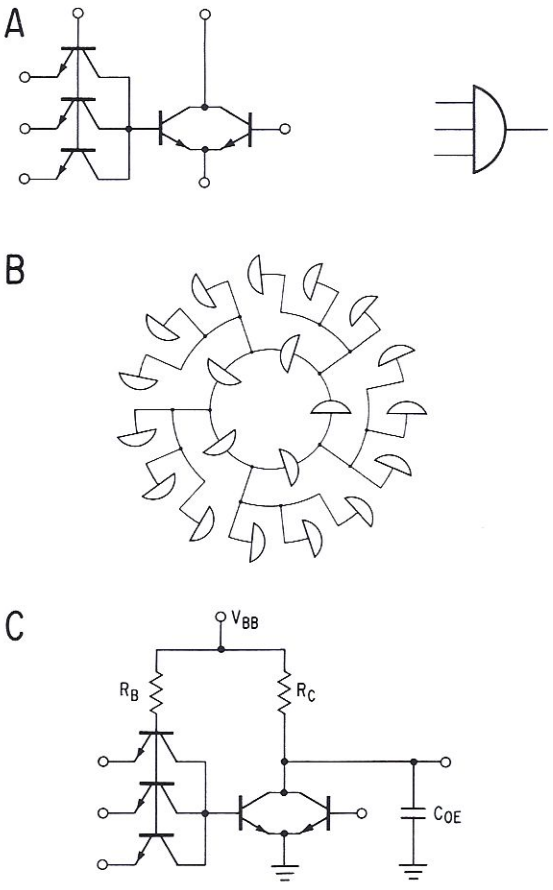

Fig. 5. Ring oscillator for studying fan-out and capacitance effects on delay. a) schematic of FSP-352-1, b) block diagram, and c) parameters of interest.

Some of the parameters of interest are shown in Figure 5c. V_{BB} is the supply voltage. For a given node current, the power consumed per node is proportional to the supply voltage. So it is desirable to know if reducing the supply from, say, six to three volts (keeping the node current constant) will have much effect on delay.

R_C is the pull-up resistor. Its purpose is to charge the load capacitance when the inverter transistor turns off, thereby decreasing the delay time. Unfortunately, it also pulls the succeeding gate transistors out of saturation, which will increase delay. Therefore, the net effect of R_C on delay is not obvious, so it is desirable that the effect of R_C be measured.

C_{OE} represents the capacitance added by loads separate from the fan-out loads expected. Wiring, measurement instruments, and read-out circuits would contribute to this capacitance.

F_O stands for fan-out, t_{pd} the average propagation delay, and I_{N1} the on node current, that is, the current through R_B when the inverter is conducting.

Curves drawn from measurements made with the ring oscillator are shown in Figures 6 through 9, and are discussed in the following paragraphs.

Effect of Fan-Out

For node currents below one milliampere, increasing the fan-out decreases the delay time, as shown in Figure 6. This is probably due to a combination of two effects. As fan-out increases, collector current increases, which means the current gain also increases. At about one milliampere node current, the current gain is maxi-

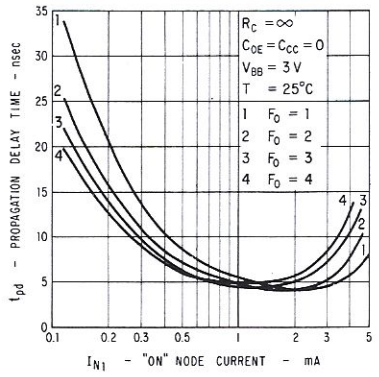

Fig. 6. Ring oscillator node currents vs delay time with various fan-outs.

mum. The second effect is that excess base current is reduced as fan-out increases, which will decrease storage time during turn-off. Above one milliampere node current, the current gain of the 2N709 begins to decrease.

Effect of Supply Voltage

Figure 7 shows that reducing the supply from 6 to 3 volts does not significantly affect delay time at one milliampere on node current. From one-fourth to one or two milliamperes the decrease in supply actually improves the delay times. Below one-fourth of a milliampere, the larger supply voltage yields the best delay times, the improvement increasing as current decreases.

Effect of "Pull-Up" Resistance

Figures 8 and 9 show that the use of a collector resistor degrades the delay times except at low currents, where there is little or no difference. In other words, pulling the gate transistor out of saturation with a collector resistor increases the delay more than charging the collector-emitter capacitance with the resistor decreases the delay. Since the collector resistor increases the power dissipation about fifty percent without any improvement in delay times, it should not be used.

LOGIC CIRCUITS USING T^2L

Both AND and OR functions are available using the basic T^2L NAND gate, as shown in Figure 10a. This meets one of the design goals mentioned at the beginning of the paper.

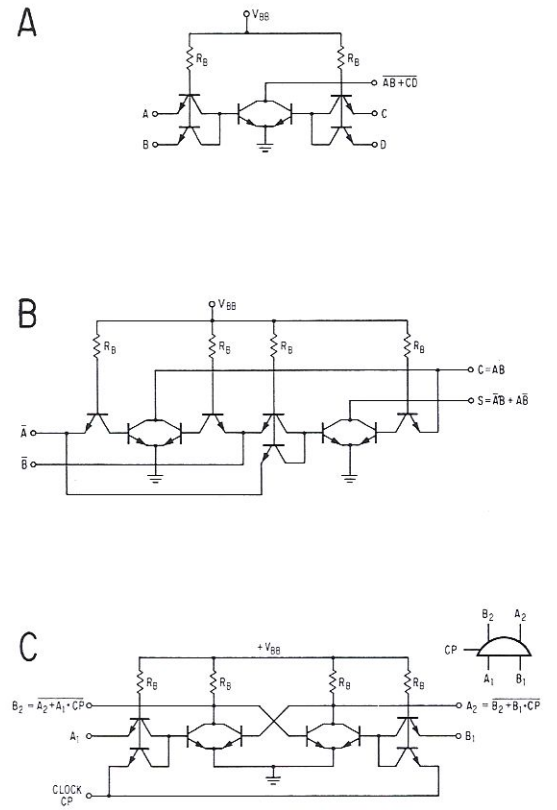

Fig. 10. AND and OR functions using T^2L. a) NAND gate, b) half adder, c) DCTL flip-flop.

A half adder circuit is shown in Figure 10b. If both the AND and the OR functions were not available, three separate gates would be required which would increase the delay through the circuit by 50%.

A DCTL flip-flop with T^2L gating is shown in Figure 10c.

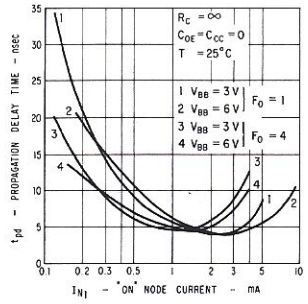

Fig. 7. Ring osc. I_{N1} vs t_{pd} with various supply voltages.

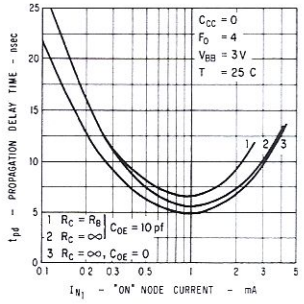

Fig. 8. Ring osc. I_{N1} vs tpd with various R_C and C_{OE} at 3 volts supply.

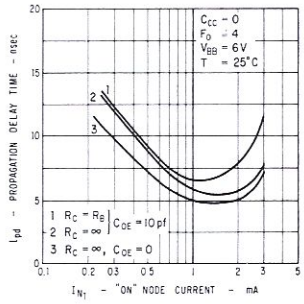

Fig. 9. Ring osc. I_{N1} vs t_{pd} with various R_C and C_{OE} at 6 volts supply.

T^2L Decimal Counter

Five such flip-flops were used to build a decimal counter; the block diagram is shown in Figure 11. The truth table in Figure 11 uses positive logic; that is, a one is represented by a positive voltage, and a zero is represented by a voltage near ground. Assume all lettered outputs are initially zero. The next positive going clock pulse will not affect any flip-flops except A because they are already in the state to which the clock pulse would advance them. For example, a clock pulse could enter only the left side of flip-flop C because B holds the gate at the right side of B off. So the clock pulse will tend to make C a zero, which it already is. This is also true of flip-flops B, D, and E. However, the state of flip-flop E will enable the clock pulse to turn on the right side of flip-flop A, making it a zero, which changes A to a one. For the same reasons the second clock pulse will change only flip-flop B, the third will change only flip-flop C, and so on. After ten clock pulses, all flip-flops will be in the same conditions as before the first clock pulse. That is, each flip-flop will have divided the input repetition rate by ten.

If a clock pulse is too long, more than one flip-flop will change states during one clock pulse because the entire counter is direct-coupled. Therefore, if all the clock inputs are connected together, the clock pulse cannot be longer than some maximum width. At frequencies near the maximum repetition rate, a sine wave clock input meets this requirement. At lower frequencies (about half the maximum repetition rate and below) the clock input of each flip-flop may be split internally and a binary counter used to trigger the flip-flops. This is shown in Figure 12.

The decimal counter of Figure 11 was built using FSP-352-1's with R_B = 680 ohms and V_{BB} = 3 V (I_{N1} = 2 mA), giving a total power dissipation of less than 200 milliwatts. The maximum repetition rate is at least 140 mc from -55°C to +100°C, and at 25°C the maximum repetition rate is 150 mc.

CP	A	B	C	D	E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

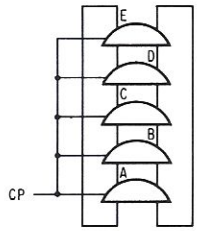

Fig. 11. Decimal counter built with FSP-352-1's operates at 150 mc.

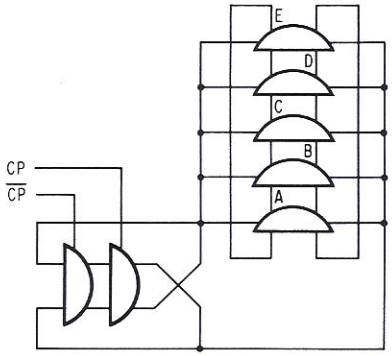

Fig. 12. Flip-flop triggered by a binary counter.

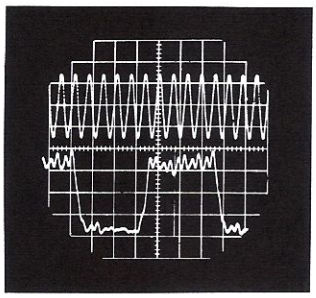

Fig. 13. Clock input and output waveforms of decimal counter (Fig. 11).

It is significant that two decimal counters using identical circuits were built with individual transistors in TO-18 cases and in each case the maximum repetition rate was only 80 mc. The size reduction made possible with multiple packaging reduced physical size, which reduced wire inductance and stray capacitance, permitting substantially increased operating frequency.

NOISE SUSCEPTIBILITY

The noise susceptibility of digital circuitry is usually reduced by reverse biasing the base-emitter junctions of the non-conducting transistors. This cannot be done with T^2L circuitry, as shown in Figure 14. As soon as I_{BB} is large enough to make $V_{BE(off)}$ less than $V_{CE(sat)}$ by about ten millivolts, the gate transistor will go from the saturated region to the inverted active region. Since inverted current gain is very small, the reverse biasing current will nearly equal the off node current.

$$I_{BB} \geq I_{N2}$$

Since I_{N2} is greater than I_{N1}, when T1 turns off, the sink providing I_{BB} takes all the node current, and there is no current for the base of T3. Thus T3 never conducts.

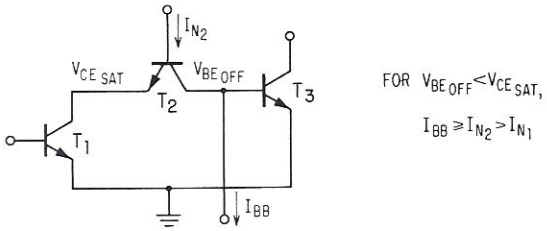

Fig. 14. T^2L circuitry showing effect of I_{BB} on $V_{BE(off)}$ disallowing reverse bias.

The noise margin of T^2L as a function of temperature may easily be calculated.

for I_{N1} = 1 mA, V_{BB} = 3 V,
F_O = 4: $I_C \approx 5.6$ mA

$V_{CE(sat)} \approx$ 210 mV @ 25°C (use 240 mV)
temp. coef. ≈ +0.8 mV/°C

$V_{CE(sat)}$ @ I_C = 0 ≈ 80 mV (use 100 mV)
temp.coef. ≈ +0.17 mV/°C

V_{BE} @ I_C = 100 μA ≈ 680 mV (use 660 mV)
temp. coef. ≈ -1.8 mV/°C

noise margin ≥ (660 - 240 - 100) mV -

(T-25°C) (1.8 + 0.8 + 0.17) mV

noise margin ≥ 320 mV - (2.77 mV/°C)(T-25°C)

This curve is plotted in Figure 15. The noise margin for T^2L is less than that to which digital circuit designers have become accustomed. However, T^2L uses less current than that to which digital circuit designers have become accustomed, which reduces noise margin requirements.

The use of a high speed epitaxial transistor, such as type 2N2368 or 2N2369, will permit operation at larger currents with an equal or greater noise margin. Operation of this type of transistor at low collector currents (3 mA or less) is not recommended because their lower $V_{BE(sat)}$ will reduce the noise margin. High speed epitaxial transistors should not be used for gating, however, because of their larger inverse current gain.

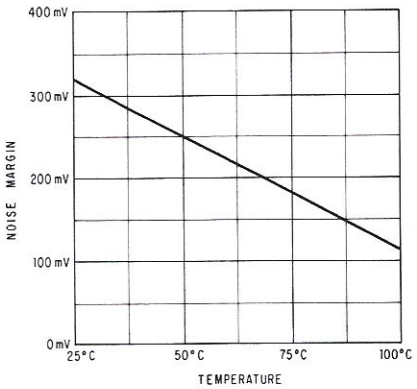

Fig. 15. Noise margin of T^2L as a function of temperature.

One of the main causes of noise in a digital system is ground currents. A wire has inductance, and if the current in the wire is changed, a voltage drop proportional to the rate of change of current will appear across the ends of the wire. For example, a wire five feet long might have an inductance of 0.5 microhenry, and if the current in the wire is changed by 20 milliamperes in 10 nanoseconds, the voltage drop will be:

$$e \approx L\frac{\Delta i}{\Delta t} = \frac{0.5 \times 10^{-6} \times 20 \times 10^{-3}}{10 \times 15^{-9}} = 1.0 \text{ Volt}$$

One volt pulses ten nanoseconds long will trigger the logic circuits described in this paper. To prove this, the circuit of Figure 16 was built. When switch S (a transistor) is closed, a current pulse flows in the wire from the emitter of T1 to the emitter of T3, making the emitter of T1 positive with respect to the emitter of T3. Since there is no change in current in the wire from the collector of T1 to the emitter of T2, the base emitter voltage of T3 becomes large enough to turn T3 on when it was supposed to remain off.

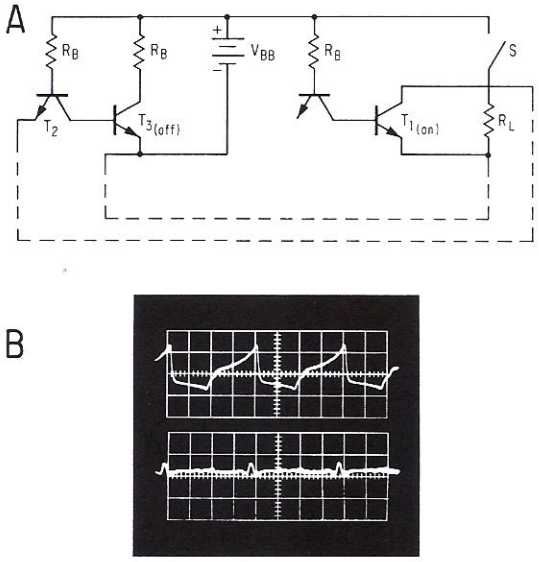

Fig. 16. a) Circuit to demonstrate the effect of ground currents, b) reduction of noise pulses by using shielded wire connections.

The collector of T1 was then connected to the emitter of T2 with RG 187/U, 75 ohm shielded wire, instead of ordinary bus wire. The shield at the end near T1 was connected to the emitter of T1, and the shield at the end near T2 was connected to the emitter of T3. The reduction in noise pulses is shown in Figure 16. The shielded wire reduced the noise from 1.6 to .04 volt pulses. Transistor T3 obviously remained off. The penalty paid is the time delay along the shielded wire. RG 187/U was selected because of its size, being only 0.1 inch in diameter.

SUMMARY OF T^2L FEATURES

1. Simplicity of only two kinds of parts and only one power supply.
2. Forms both the logical OR and the logical AND functions with common polarity.
3. Dissipates only 3 milliwatts per gate for 5 nanosecond average propagation delay under the practical operating conditions of fan-out and load capacitance.
4. Dissipates only 300 microwatts per gate for less than 25 nanoseconds average propagation delay under practical operating conditions, making high speed microwatt logic circuits possible.
5. Forms larger logic circuits such as a 140 megacycle decimal counter.
6. Fan-out is limited primarily by current-robbing in worst case design.
7. Noise margin is smaller than most other forms of logic but at the same time it uses less current, reducing noise margin requirements. The use of shielded wire greatly reduces the effect of ground wire noise due to inductance.

ACKNOWLEDGEMENT

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